REMARKS

Reconsideration and further examination of the application, as amended, are requested. All objections and rejections are respectfully traversed.

In the Office Action, claims 1-3, 5-7 and 9-14 were rejected under 35 U.S.C. §102 as being anticipated by U.S. Pat. No. 6,314,150 to Vowe (hereinafter "Vowe"). Claims 4 and 8 were rejected under 35 U.S.C. §103 as being obvious based on Vowe in view of U.S. Pat. No. 5,822,317 to Shibata (hereinafter "Shibata"). Applicant respectfully traverses the rejection for the reasons stated herein.

Claim 1 in relevant part recites:

> "An error detection system for **a clock signal** comprising:
>
> a first counter that receives and counts the clock signal,
>
> a phase-locked loop circuit **that receives the clock signal and outputs a second clock signal,**
>
> a second counter that receives and counts the second clock signal,
>
> a comparator that receives and compares the outputs of the first and the second counters".

As shown, claim 1 explicitly recites that a phase-locked loop (PLL) circuit receives a first clock signal, and then outputs a second clock signal. Such an arrangement is nowhere disclosed in Vowe. In fact, Vowe does not even show a PLL circuit in any of his figures. Instead, as shown in Fig. 2, Vowe discloses a lock detection circuit (LD) that receives two signals, TA and TB. The first signal, TA, corresponds to the divided-down output signal of a phase-locked loop. See Col. 5, lines 48-50 ("The first input clock sig-

nal TA may be, for example, the divided-down output clock signal of the phase-locked loop"). The phase-locked loop circuit that generates TA is nowhere shown in any of Vowe's figures. The second clock signal, TB, is the reference clock signal. See Col. 5, lines 50-51.

To sustain a rejection under §102, the cited reference must disclose each and every element of the corresponding claim, and the reference must show those elements arranged in the same way as the claim recites. See MPEP §2131. As explained above, Vowe fails to disclosure a phase-locked loop that **receives a first clock signal** and outputs a second clock signal that is then received by a second counter. Instead, Vowe simply states that his lock detector (LD) receives a divided down output of a phase-lock loop. Because Vowe fails to disclose a phase-locked loop circuit that "receives [a first] clock signal and outputs a second clock signal", the rejection of claim 1 based on Vowe should be withdrawn.

Independent claims 5 and 9 are also distinguishable over Vowe. In particular, claim 5 in relevant part recites:

> "A method for detecting clock signal errors comprising the steps of:",
>
> "a first counting of the first clock signals", and
>
> "providing a second clock signal **with a frequency that is locked to the average frequency of the first clock signal**".

As shown above, Vowe fails to provide any disclosure for a second clock signal that is "locked to the average frequency of the first clock signal". Indeed, Vowe provides no disclosure any relationship between his two clock signals, TA and TB.

Similarly, claim 9 in relevant part recites:

"A system for detecting errors in a first clock signal, the system comprising:"

"means for counting the first clock signal," and

"means, **responsive to the first clock signal**, for generating a second clock signal".

Again, Vowe fails to provide any disclosure of a second clock signal that is responsive to a first clock signal. Accordingly, the rejections of claims 5 and 9 based on Vowe should be withdrawn.

Claims 2-4, 6-8 and 10-14 depend from claims 1, 5 and 9, and thus they too are in condition for allowance for these as well as other reasons.

For example, claim 2 recites:

> "The error detection system as defined in claim 1 further comprising **a second output from the comparator that indicates which counter contains a higher count.**"

Vowe fails to disclose such a second output from a comparator. Instead, Vowe's two comparators, VA and VB, output a Boolean indication (i.e., a "1" or a "0"), and reset signals (i.e., RESET_A and RESET_B). Vowe provides no disclosure for a comparator that includes, as one of its outputs, an indication as to which of two different counters had a higher count. Nonetheless, the Office Action relies on Vowe to reject claim 2 contending that "Vowe inherently discloses an output from the comparator that indicates which counter contains a higher count".

The Office Action, however, fails to satisfy its burden in rejecting claim 2 based on inherency. As noted in the MPEP, the Federal Circuit has ruled that:

> "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the ref-

> erence, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'"

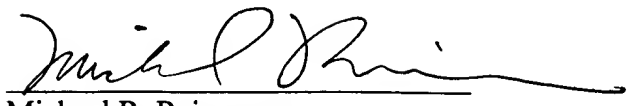
MPEP §2112, quoting In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999). Here, no extrinsic evidence has been cited in the Office Action in support of the contention that Vowe's comparator inherently provides, as an output, an indication of which counter contains a higher count. Furthermore, just because Vowe discloses a comparator does not mean that Vowe's comparator must also indicate which counter has the higher count. Indeed, all Vowe ever describes is that his comparator indicates when the two counters differ. Thus, there is no suggestion by Vowe to provide an output from his comparator that indicates which of the counters has the higher count, and no extrinsic evidence has been identified by the Office Action. Accordingly, the rejection of claim 2, which is based on inherency, should be withdrawn.

New claims

Applicant has amended the claims to add new claims 15 and 16. No new matter is being introduced. More specifically, new claims 15 and 16 are similar to previously presented claims 13 and 10, but with different dependencies.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Respectfully submitted,



Michael R. Reinemann
Reg. No. 38,280
(617) 951-2500

Send all correspondence to:

IP Administration Legal Department,
M/S 35
Hewlett-Packard Co.
P.O. Box 272400
Fort Collins, CO 80527-2400